PIPELINED INSTRUCTION DISPATCH UNIT IN A SUPERSCALAR PROCESSOR

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ABSTRACT OF THE DISCLOSURE

A pipelined instruction dispatch or grouping circuit allows instruction dispatch decisions to be made over multiple processor cycles. In one embodiment, the grouping circuit performs resource allocation and data dependency checks on an instruction group, based on a state vector which includes representation of source and destination registers of instructions within said instruction group and corresponding state vectors for instruction groups of a number of preceding processor cycles.